

Direct Sequence Spread Spectrum Physical Layer Specification IEEE 802.11

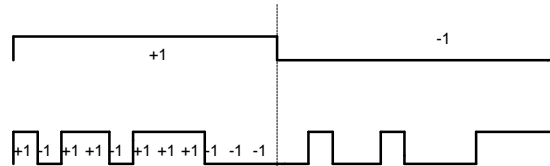
Prepared by Jan Boer, Chair DS PHY
Lucent Technologies WCND Utrecht

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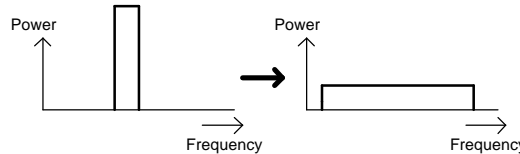
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What is DSSS?

- Signal symbol is spread with a sequence



- Wider Bandwidth
- Less power density

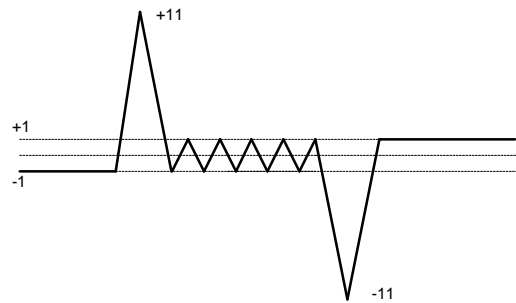


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11 chip BARKER sequence

- Good autocorrelation properties
- Minimal sequence allowed by FCC
- Coding gain 10.4 dB

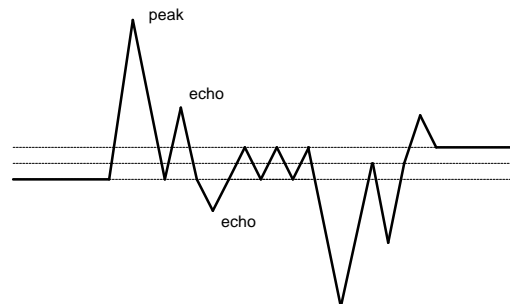


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DSSS benefits

- 10 dB coding gain:
 - Robust against interferers and noise (10 dB suppression)
- Robust against time delay spread
 - Resolution of echoes



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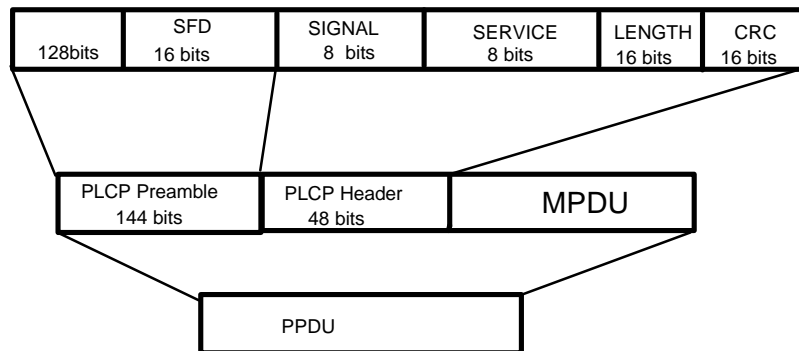
IEEE 802.11 DSSS PHY characteristics

- 2.4 GHz ISM band (FCC 15.247)
- 1 and 2 Mb/s datarate (DBPSK and DQPSK modulation)
- Symbolrate 1MHz
- Chipping rate 11 MHz with 11 chip Barker sequence
- Multiple channels in 2.4 to 2.4835 GHz band

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PLCP Frame Format

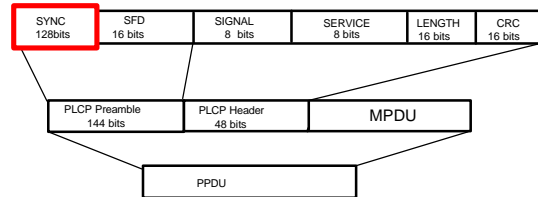


Preamble and Header always at 1Mb/s DBPSK

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PLCP synchronization

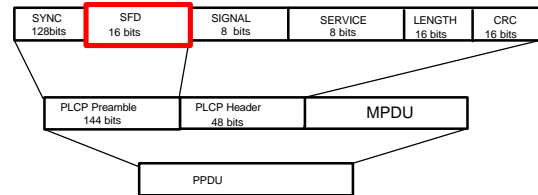


- 128 scrambled 1 bits
- needed for o.a.
 - gain setting
 - energy detection
 - antenna selection
 - frequency offset compensation

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Start Frame Delimiter

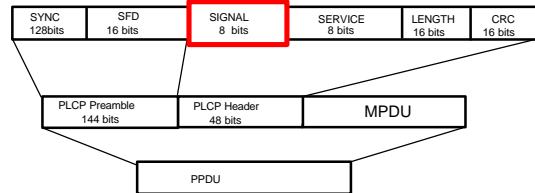


- 16 bit field (hF3A0)
- used for
 - bit synchronization

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Signal Field

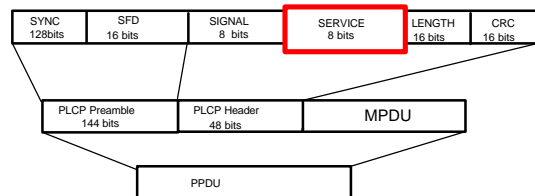


- Rate indication
 - h0A 1Mb/s DBPSK
 - h14 2Mb/s DQPSK
- Other values reserved for future use (100 kb/s quantities)

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Service Field

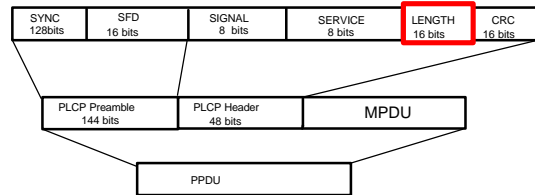


- Reserved for future use
- h00 signifies 802.11 compliant

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Length Field

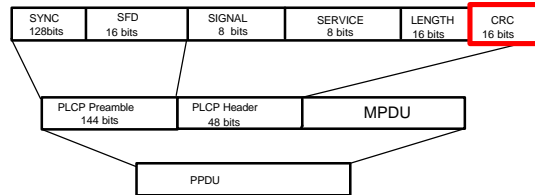


- Indicates number of octets to be transmitted in MPDU
- Used for
 - End of frame detection
 - MPDU CRC sync

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CRC field



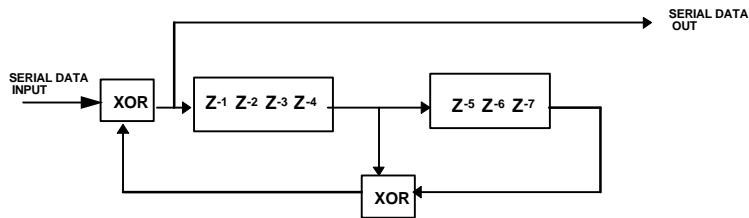
- CCITT CRC-16
- Protects Signal, Service and Length Field

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Data Scrambler

Scrambler Polynomial; $G(z)=Z^{-7} + Z^{-4} + 1$

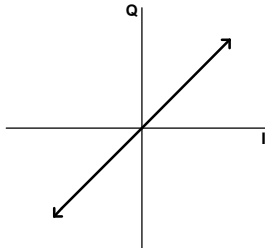


- ALL bits transmitted by the DSSS Phy are scrambled
- Purpose
 - Whithening the spectrum
 - DC blocking (Barker sequece is asymmetric)

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DBPSK Modulation



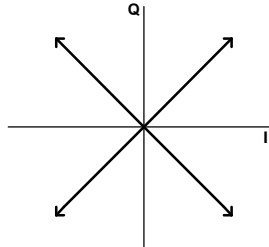
Bit Input	Phase Change (+jω)
0	0
1	π

Table 1, 1 Mb/s DBPSK Encoding Table.

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DQPSK Modulation



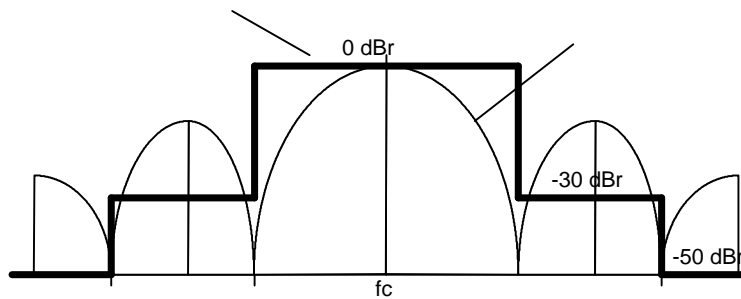
Dibit pattern (d0,d1) d0 is first in time	Phase Change (+jω)
00	0
01	$\pi/2$
11	π
10	$3\pi/2$ ($-\pi/2$)

Table 1, 2 Mb/s DQPSK Encoding Table

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Transmit Spectrum Mask



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DSSS Channels

CHNL_ID	FCC Channel Frequencies	ETSI Channel Frequencies	Japan Frequency
1	2412 MHz	N/A	N/A
2	2417 MHz	N/A	N/A
3	2422 MHz	2422 MHz	N/A
4	2427 MHz	2427 MHz	N/A
5	2432 MHz	2432 MHz	N/A
6	2437 MHz	2437 MHz	N/A
7	2442 MHz	2442 MHz	N/A
8	2447 MHz	2447 MHz	N/A
9	2452 MHz	2452 MHz	N/A
10	2457 MHz	2457 MHz	N/A
11	2462 MHz	2462 MHz	N/A
12	N/A	N/A	2484 MHz

Table 1, DSSS PHY Frequency Channel Plan

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Clear Channel Assessment

- Three methods:
 - CCA mode 1: Energy above threshold
 - CCA mode 2: Carrier sense only
 - CCA mode 3: Carrier sense with energy above threshold
- Energy detection function of TX power
 - Tx power > 100 mW: -80 dBm
 - Tx power > 50mW : -76 dBm
 - Tx power <= 50mW: -70 dBm
- Energy detect time : 15 μ s
- Correct PLCP header --> CCA busy for full (intended) duration of of frame as indicated by PLCP Length field

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DSSS Specification Summary

- Slottime 20 μ s
- TX to Rx turnaround time 10 μ s
- Rx to Tx turnaround time 5 μ s
- Operating temperature range
 - type 1: 0 - 40 °C
 - type 2: -30 - 70 °C
- Tx Power Levels
 - 1000 mW USA
 - 100 mW Europe
 - 10 mW/MHz Japan
- Minimum Transmitted Power 1 mW
- Tx power level control required above 100 mW

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DSSS Specification Summary (cont)

- Tx Center Frequency Tolerance +/- 25 ppm
- Chip Clock Frequency Tolerance +/- 25 ppm
- Tx Power On Ramp 2 μ s
- Tx Power Down Ramp 2 μ s
- RF Carrier suppression 15 dB
- Transmit modulation accuracy test procedure
- Rx sensitivity -80 dB
@ 0.08FER (1024 Bytes)
- Rx max input level -4 dB
- Rx adjacent channel rejection >35 dB
@ > 30 MHz separation
~~between channels~~

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